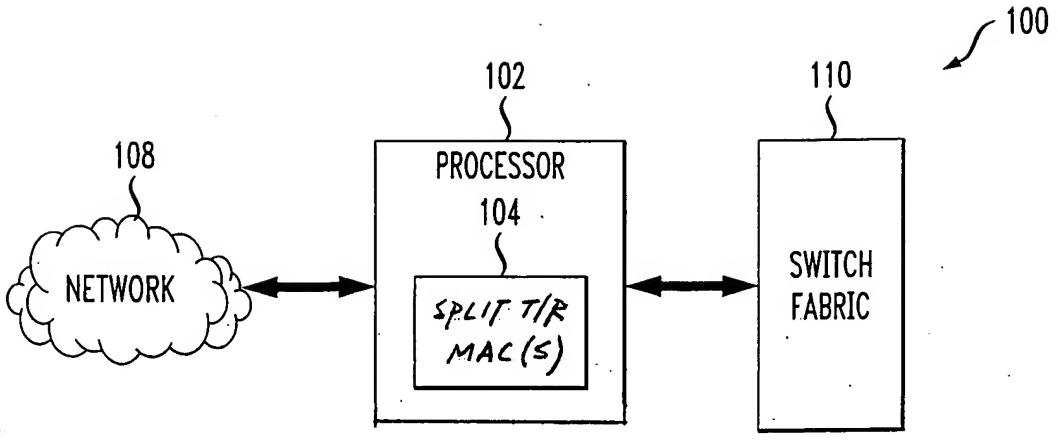
100
102
110
108
PROCESSOR
104
NETWORK
SPLIT T/R MAC(S)
SWITCH FABRIC

FIG. 1

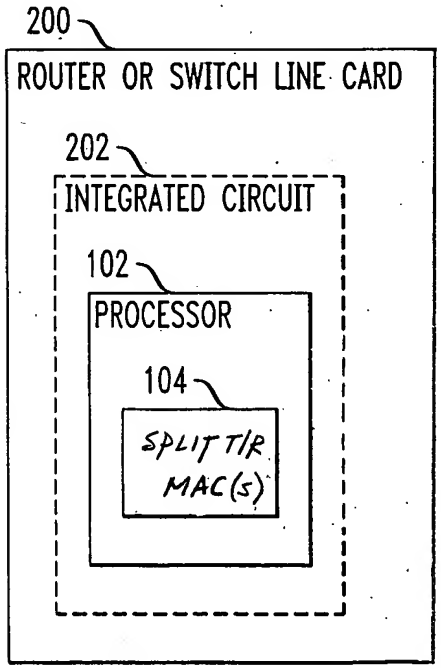
200
ROUTER OR SWITCH LINE CARD
202
INTEGRATED CIRCUIT
102
PROCESSOR
104
SPLIT T/R MAC(S)

FIG. 2

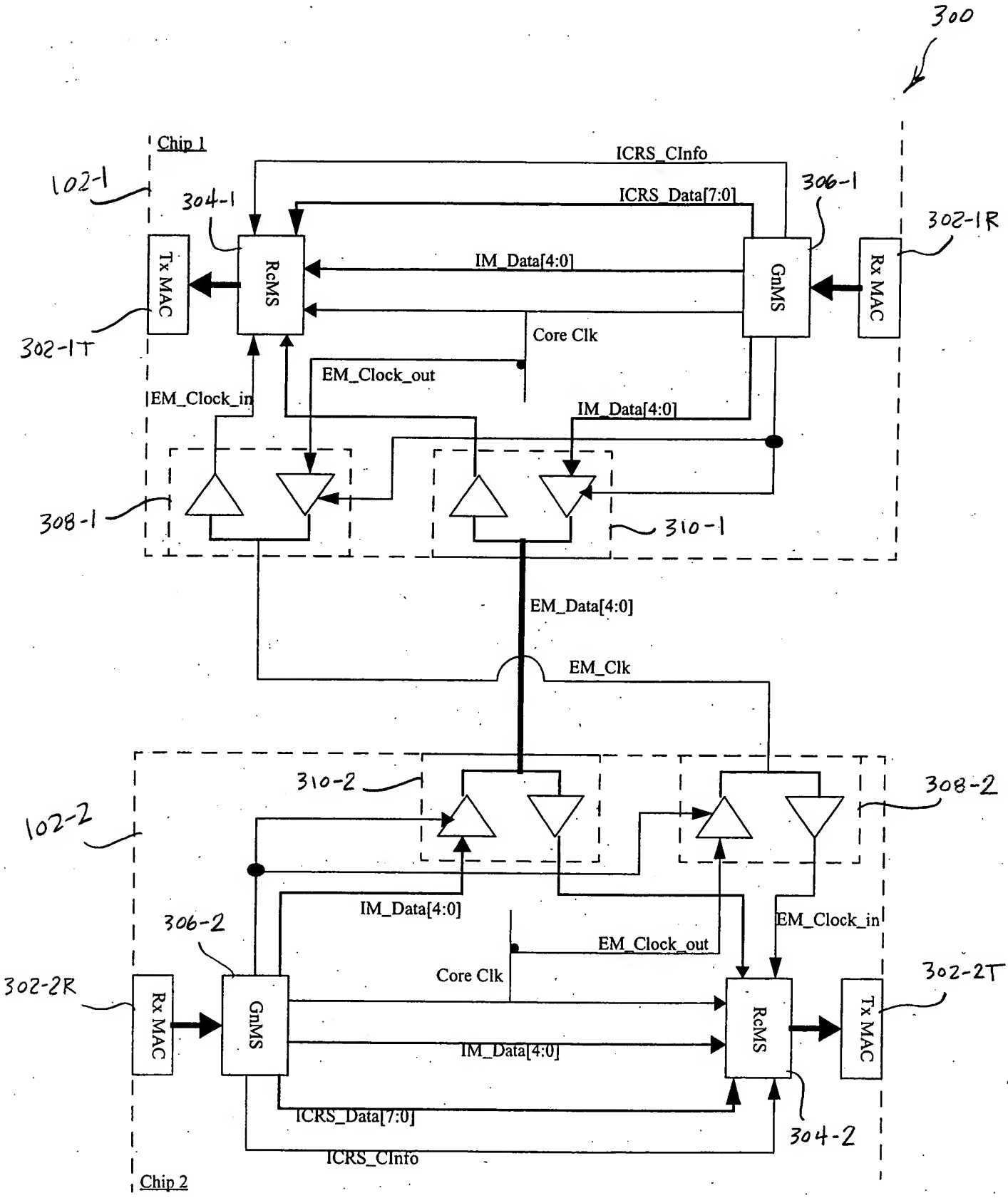
300
Chip 1
102-1
304-1
306-1
302-1R
302-1T
Tx MAC
RcMS
GnMS
Rx MAC
ICRS_CInfo
ICRS_Data[7:0]
IM_Data[4:0]
Core Clk
EM_Clock_out
EM_Clock_in
IM_Data[4:0]
308-1
310-1
EM_Data[4:0]
EM_Clk
310-2
308-2
102-2
IM_Data[4:0]
306-2
EM_Clock_out
EM_Clock_in
Core Clk
302-2R
302-2T
Rx MAC
GnMS
RcMS
Tx MAC
IM_Data[4:0]
ICRS_Data[7:0]
304-2
ICRS_CInfo
Chip 2

FIG. 3

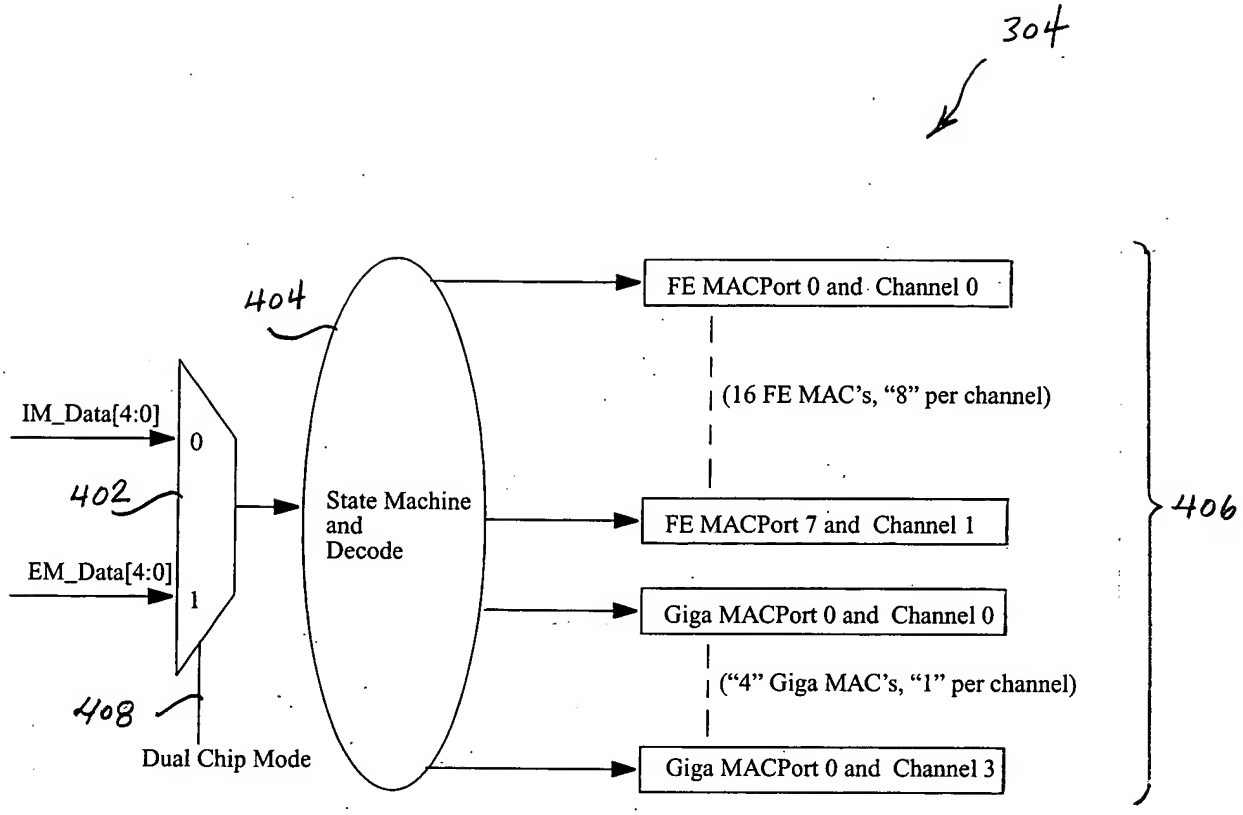
304
404
IM_Data[4:0]
0
402
EM_Data[4:0]
1
408
Dual Chip Mode
State Machine
and
Decode
FE MACPort 0 and Channel 0
(16 FE MAC's, "8" per channel)
FE MACPort 7 and Channel 1
Giga MACPort 0 and Channel 0
("4" Giga MAC's, "1" per channel)
Giga MACPort 0 and Channel 3
406

FIG. 4

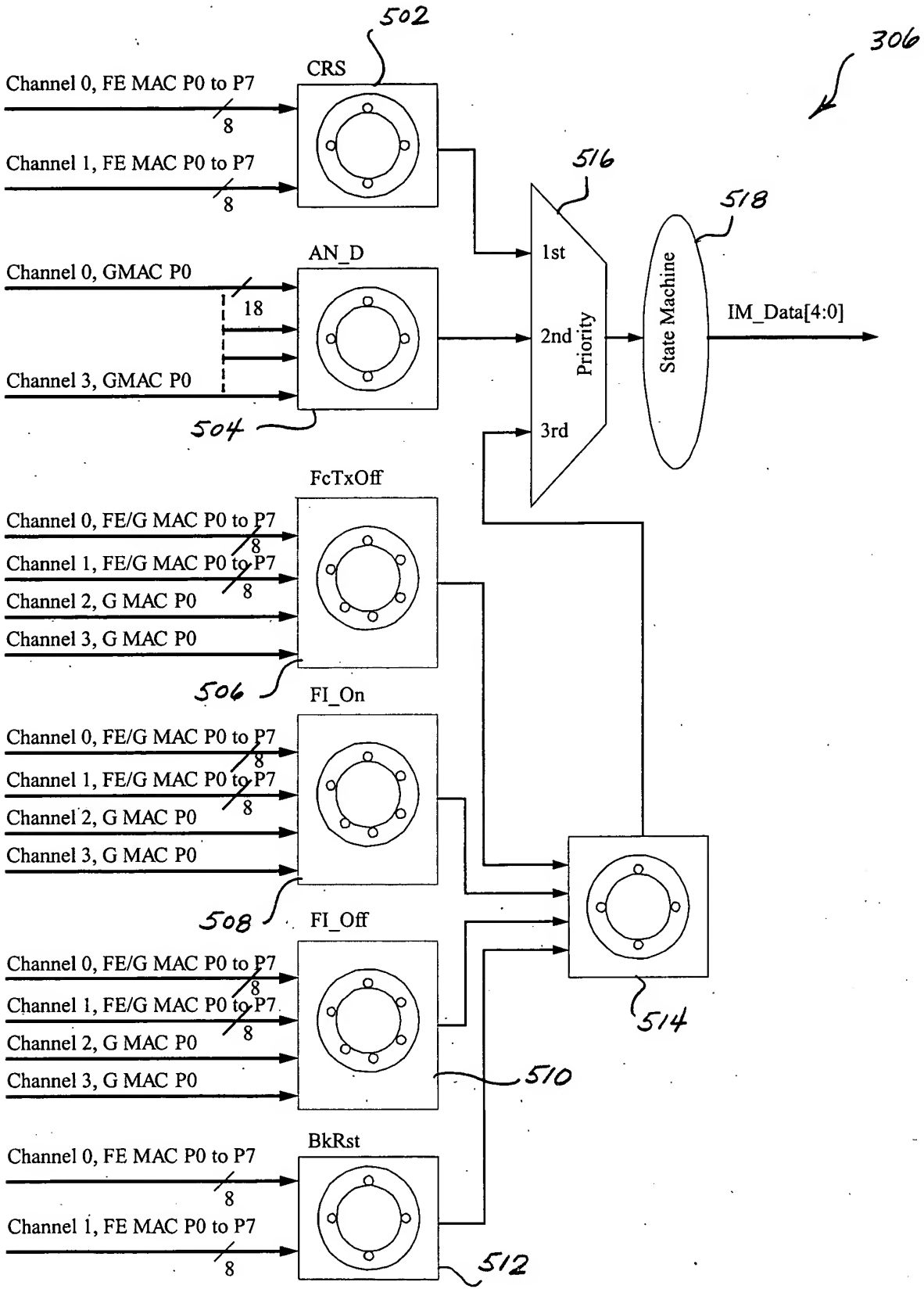
502
306
CRS
Channel 0, FE MAC P0 to P7
8
Channel 1, FE MAC P0 to P7
8
516
518
AN_D
1st
Channel 0, GMAC P0
18
2nd
Priority
State Machine
IM_Data[4:0]
Channel 3, GMAC P0
3rd
504
FcTxOff
Channel 0, FE/G MAC P0 to P7
8
Channel 1, FE/G MAC P0 to P7
8
Channel 2, G MAC P0
Channel 3, G MAC P0
506
FI_On
Channel 0, FE/G MAC P0 to P7
8
Channel 1, FE/G MAC P0 to P7
8
Channel 2, G MAC P0
Channel 3, G MAC P0
508
FI_Off
Channel 0, FE/G MAC P0 to P7
8
Channel 1, FE/G MAC P0 to P7
8
Channel 2, G MAC P0
Channel 3, G MAC P0
510
514
BkRst
Channel 0, FE MAC P0 to P7
8
Channel 1, FE MAC P0 to P7
8
512

FIG. 5

Addr decoding for CRS for FE MAC RX

Channel Addr[1:0]	Nib-ble Addr	[3:0]	Bit 0	Bit 1	Bit 2	Bit 3
00	0	CRS_C00_s	CRS_C0P0_s	CRS_C0P1_s	CRS_C0P2_s	CRS_C0P3_s
00	1	CRS_C01_s	CRS_C0P4_s	CRS_C0P5_s	CRS_C0P6_s	CRS_C0P7_s
01	0	CRS_C10_s	CRS_C1P0_s	CRS_C1P1_s	CRS_C1P2_s	CRS_C1P3_s
01	1	CRS_C11_s	CRS_C1P4_s	CRS_C1P5_s	CRS_C1P6_s	CRS_C1P7_s
10	0	CRS_C20_s	CRS_C2P0_s	CRS_C2P1_s	CRS_C2P2_s	CRS_C2P3_s
10	1	CRS_C21_s	CRS_C2P4_s	CRS_C2P5_s	CRS_C2P6_s	CRS_C2P7_s
11	0	CRS_C30_s	CRS_C3P0_s	CRS_C3P1_s	CRS_C3P2_s	CRS_C3P3_s
11	1	CRS_C31_s	CRS_C3P4_s	CRS_C3P5_s	CRS_C3P6_s	CRS_C3P7_s

FIG. 6

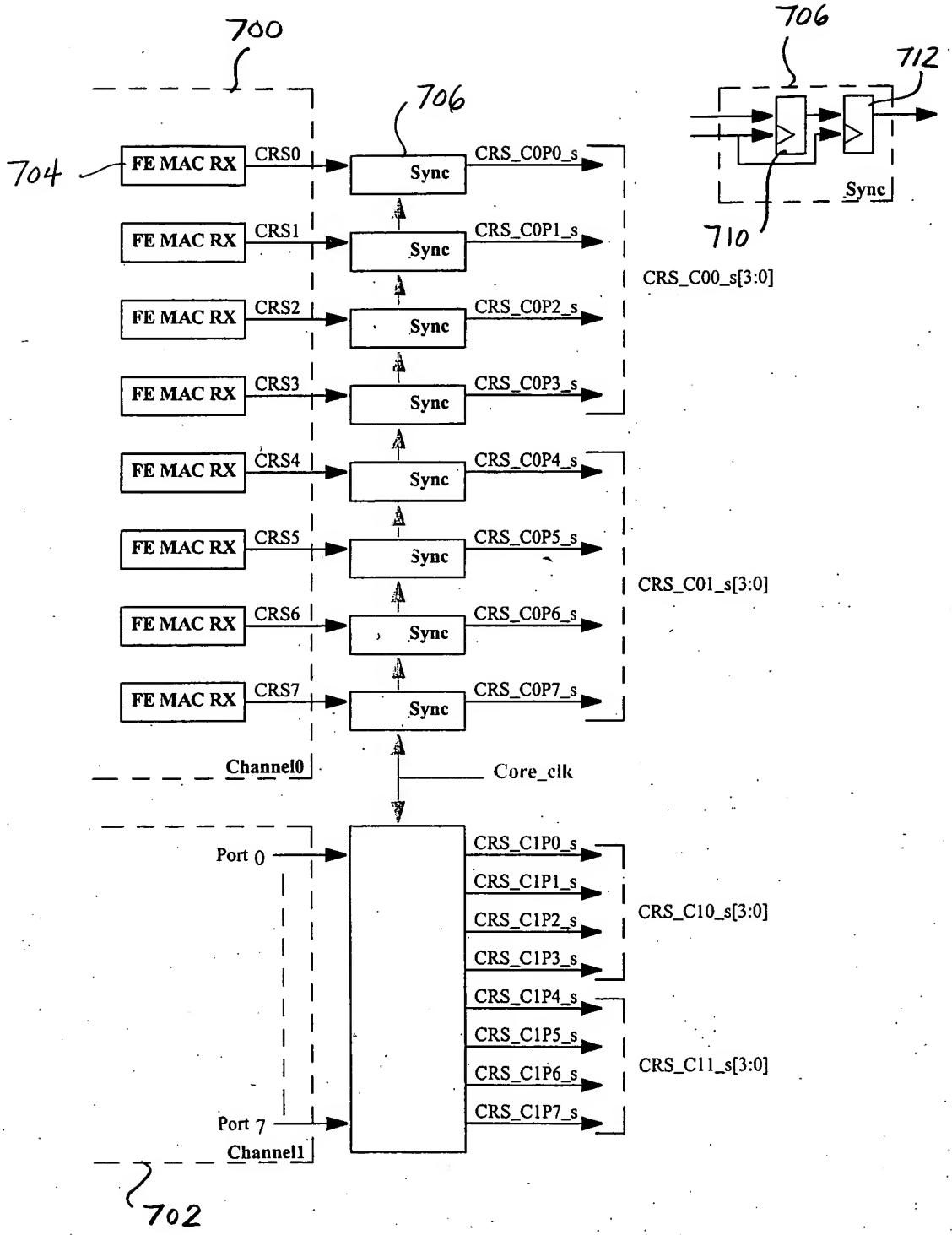
700
706
712
704
706
FE MAC RX
CRS0
Sync
CRS_C0P0_s
FE MAC RX
CRS1
Sync
CRS_C0P1_s
FE MAC RX
CRS2
Sync
CRS_C0P2_s
FE MAC RX
CRS3
Sync
CRS_C0P3_s
FE MAC RX
CRS4
Sync
CRS_C0P4_s
FE MAC RX
CRS5
Sync
CRS_C0P5_s
FE MAC RX
CRS6
Sync
CRS_C0P6_s
FE MAC RX
CRS7
Sync
CRS_C0P7_s
Channel0
Core_clk
Port 0
CRS_C1P0_s
CRS_C1P1_s
CRS_C1P2_s
CRS_C1P3_s
CRS_C1P4_s
CRS_C1P5_s
CRS_C1P6_s
CRS_C1P7_s
Port 7
Channel1
702
Sync
710
CRS_C00_s[3:0]
CRS_C01_s[3:0]
CRS_C10_s[3:0]
CRS_C11_s[3:0]

FIG. 7

Addr decoding for BkRst for 16 FE MAC RX

Channel Addr[1:0]	Nib-ble Addr	[3:0]	Bit 0	Bit 1	Bit 2	Bit 3
00	0	BkRst_C00_s	BkRst_C0P0_s	BkRst_C0P1_s	BkRst_C0P2_s	BkRst_C0P3_s
00	1	BkRst_C01_s	BkRst_C0P4_s	BkRst_C0P5_s	BkRst_C0P6_s	BkRst_C0P7_s
01	0	BkRst_C10_s	BkRst_C1P0_s	BkRst_C1P1_s	BkRst_C1P2_s	BkRst_C1P3_s
01	1	BkRst_C11_s	BkRst_C1P4_s	BkRst_C1P5_s	BkRst_C1P6_s	BkRst_C1P7_s
1X	NA	NA	NA	NA	NA	NA

FIG. 8

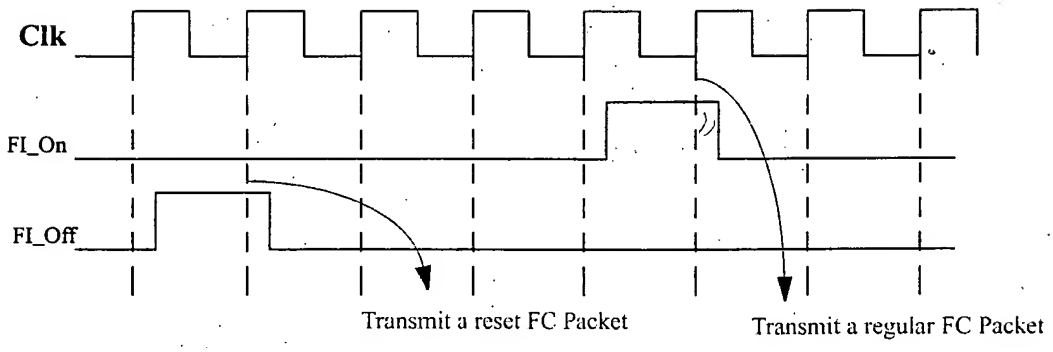
Clk
FI_On
FI_Off
Transmit a reset FC Packet
Transmit a regular FC Packet

FIG. 9

Addr decoder for A-N register information

Channel Addr[1:0]	Nib-ble Addr/ Ctrl	[3:0]	Bit 0	Bit 1	Bit 2	Bit 3
00, 01, 10, 11	0, 1	AN_D0_s	TxLreg_s[0]	TxLreg_s[1]	TxLreg_s[2]	TxLreg_s[3]
	XData_s	AN_D1_s	TxLreg_s[4]	TxLreg_s[5]	TxLreg_s[6]	TxLreg_s[7]
	Xconfig_s	AN_D2_s	TxLreg_s[8]	TxLreg_s[9]	TxLreg_s[10]	TxLreg_s[11]
	0	AN_D3_s	TxLreg_s[12]	TxLreg_s[13]	TxLreg_s[14]	TxLreg_s[15]

FIG. 10

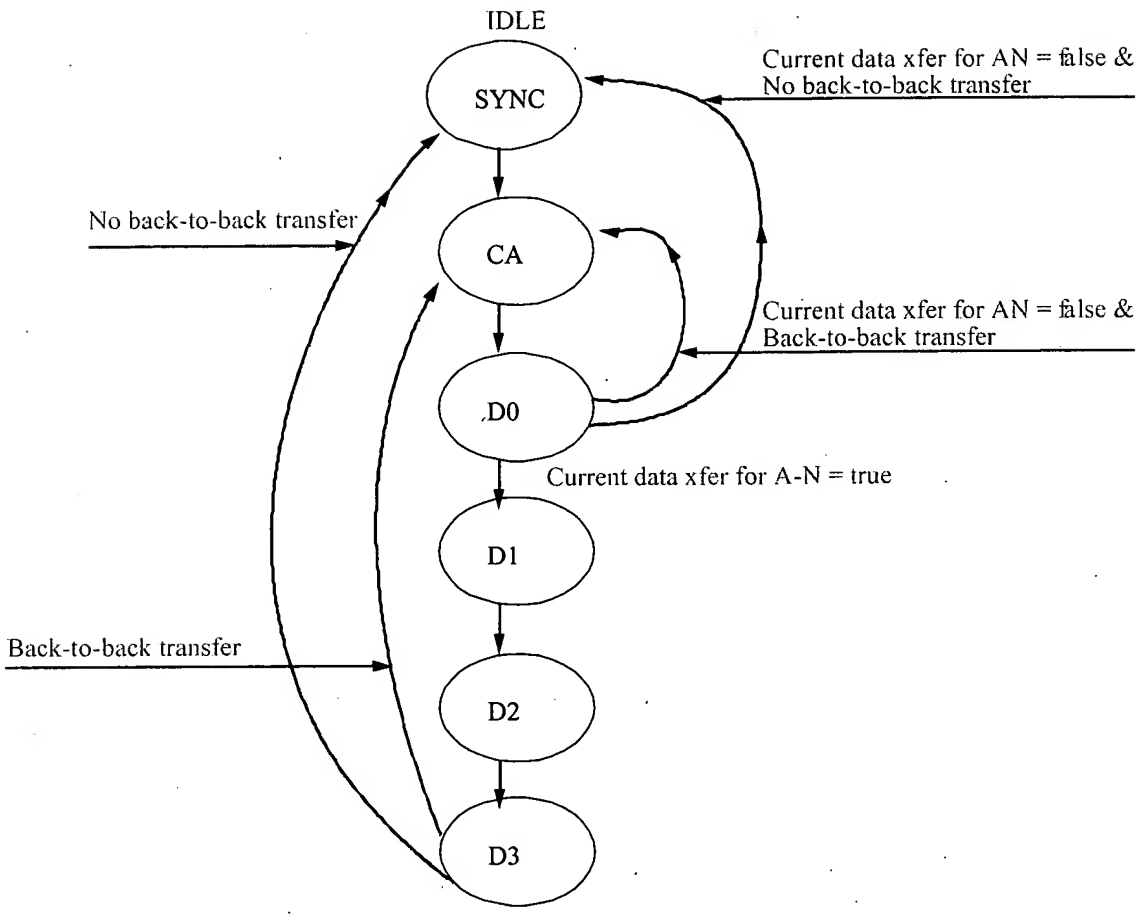
IDLE
SYNC
Current data xfer for AN = false &
No back-to-back transfer
No back-to-back transfer
CA
Current data xfer for AN = false &
Back-to-back transfer
D0
Current data xfer for A-N = true
D1
Back-to-back transfer
D2
D3

FIG. 11

Control Information Decode

Ctrl[2:0]	Control Type
3'b000	SYNC
3'b001	CRS
3'b010	AN_D
3'b011	FcTxOFF
3'b100	FI_On
3'b101	FI_Off
3'b110	BkRst
3'b111	Reserved

FIG. 12

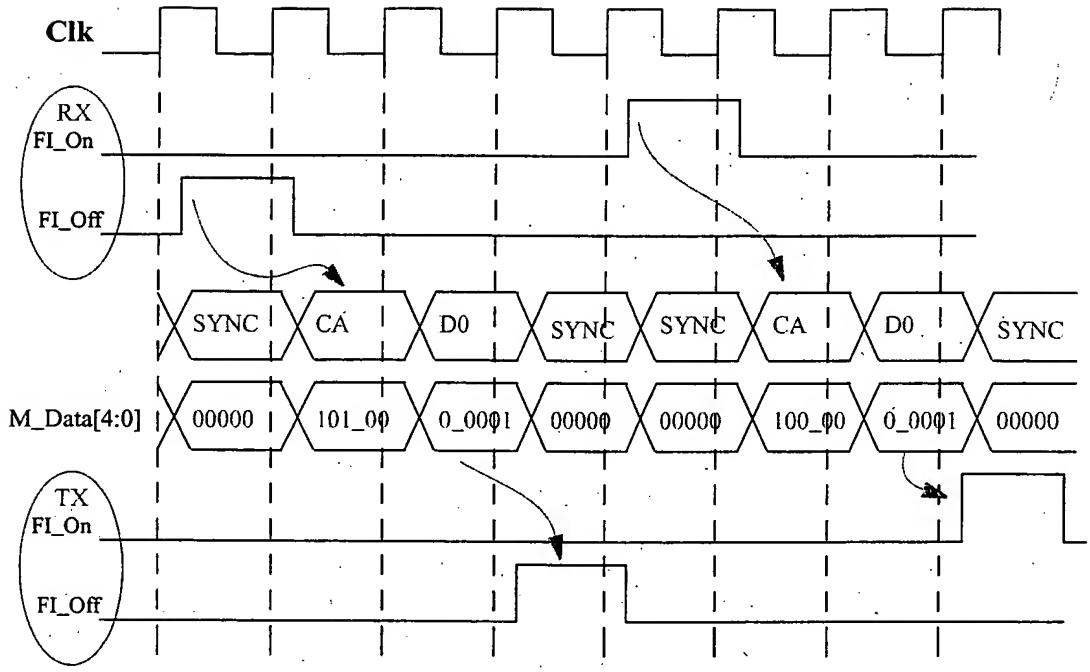
Clk
RX
FI_On
FI_Off
SYNC
CA
D0
SYNC
SYNC
CA
D0
SYNC
M_Data[4:0]
00000
101_00
0_0001
00000
00000
100_00
0_0001
00000
TX
FI_On
FI_Off

FIG. 13

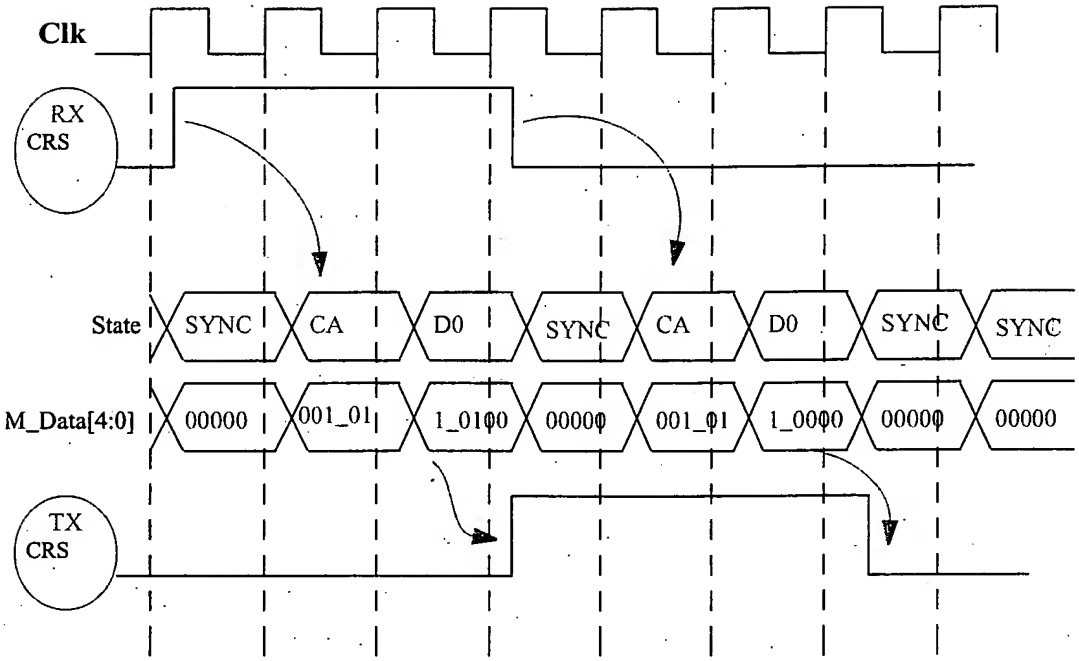
Clk
RX
CRS
State
SYNC
CA
D0
SYNC
CA
D0
SYNC
SYNC
M_Data[4:0]
00000
001_01
1_0100
00000
001_01
1_0000
00000
00000
TX
CRS

FIG. 14

Example waveform FOR T/R INTERFACE

Clock	x+1	x+2	x+3	x+4	x+5
M_Data[4:0]	5'b001_00	5'b0_1010	5'b101_10	5'b0_0001	5'b000_00
Phase	CA	Data	CA	Data	SYNC
Decoded Ctrl	CRS	NA	FI_Off	NA	NA
Channel Addr	Channel0	NA	Channel2	NA	NA
Nibble A/C	NA	0	NA	NA	NA
Data[3:0]	NA	4'b1010	NA	4'b0001	NA
		CRS_C00_s		FO_C20_s	

FIG. 15

Example for A-N info on T/R Interface for Channel 3, Nib address 0

Clock	x+1	x+2	x+3	x+4	x+5	x+6
M_Data[4:0]	5'b010_11	5'b0_1010	5'b1_0010	5'b0_1110	5'b0_1101	5'b000_00
Phase	CA	Data	Data	Data	Data	SYNC
Decoded Ctrl	A-N	NA	NA	NA	NA	NA
Channel Addr	Channel3	NA	NA	NA	NA	NA
Nibble A/C	NA	0	XData_s	XConfig_s	0	NA
Data[3:0]	NA	4'b1010	4'b0010	4'b1110	4'b1101	NA
		AN_D0_s	AN_D1_s	AN_D2_s	AN_D3_s	

FIG. 16